08/23/97 16:51:26

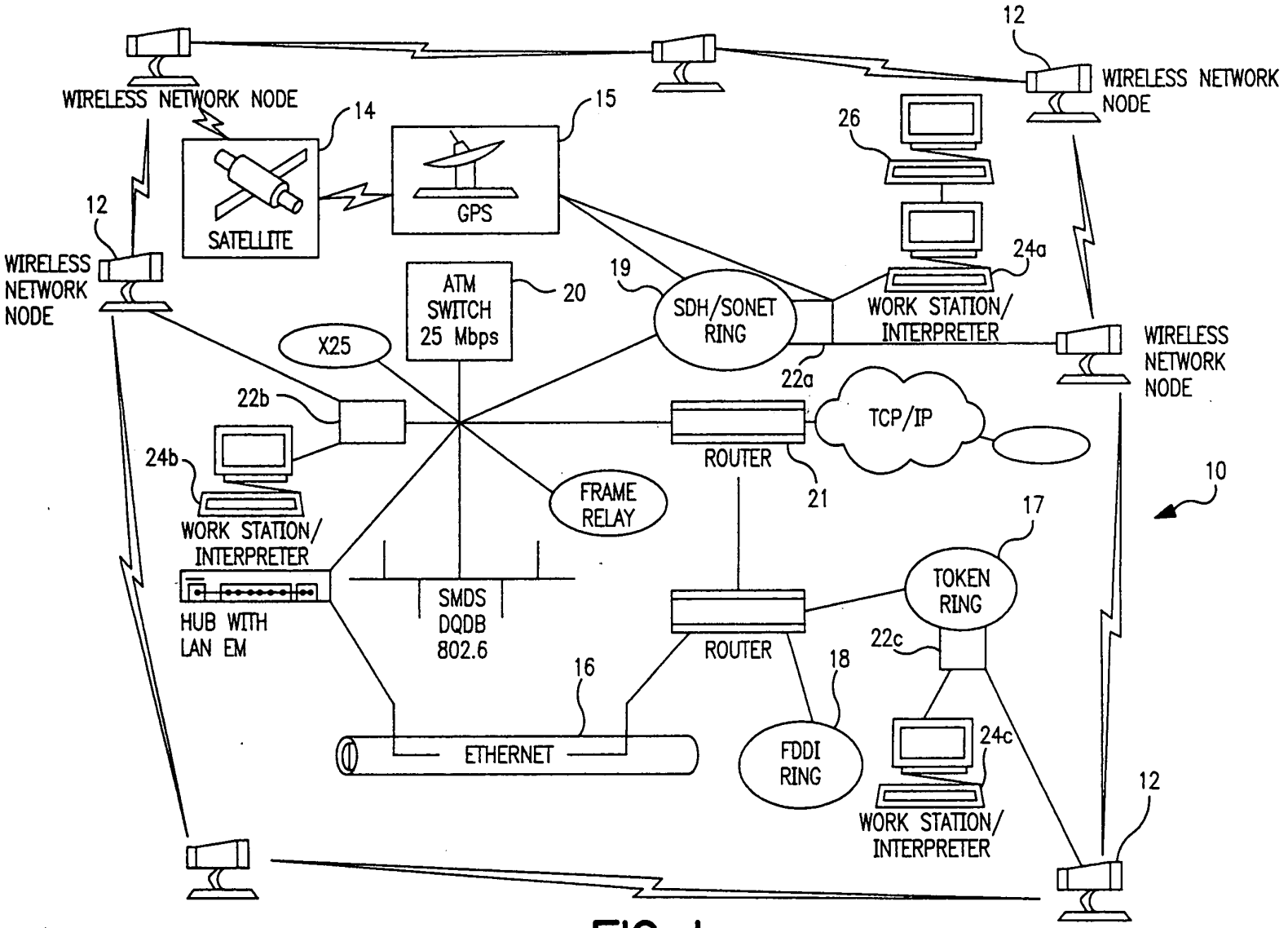

FIG. 1

PATENT APPLICATION

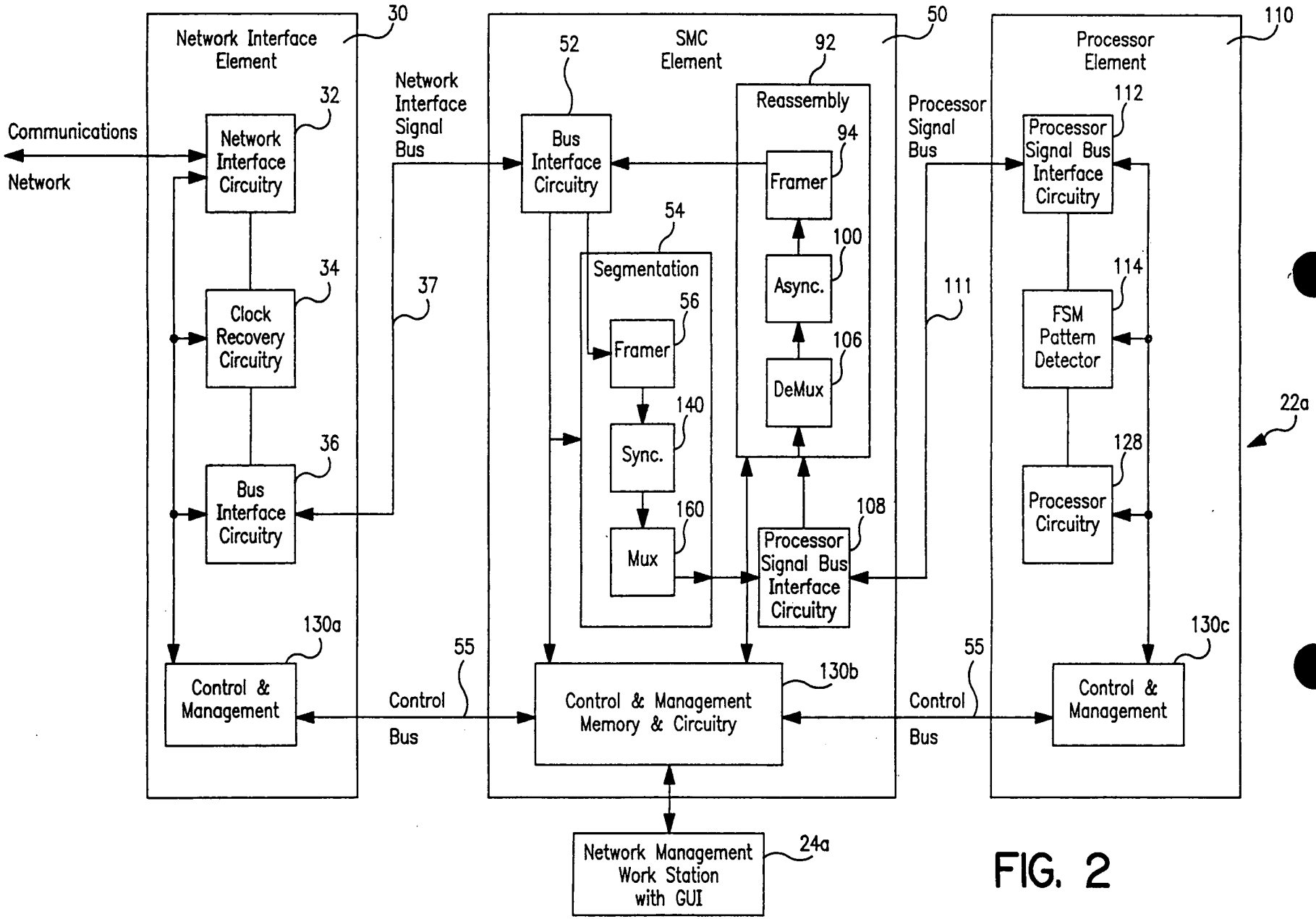

FIG. 2

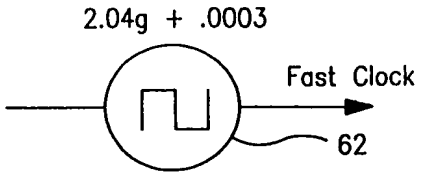
2.04g + .0003
Fast Clock
62

FIG. 3b

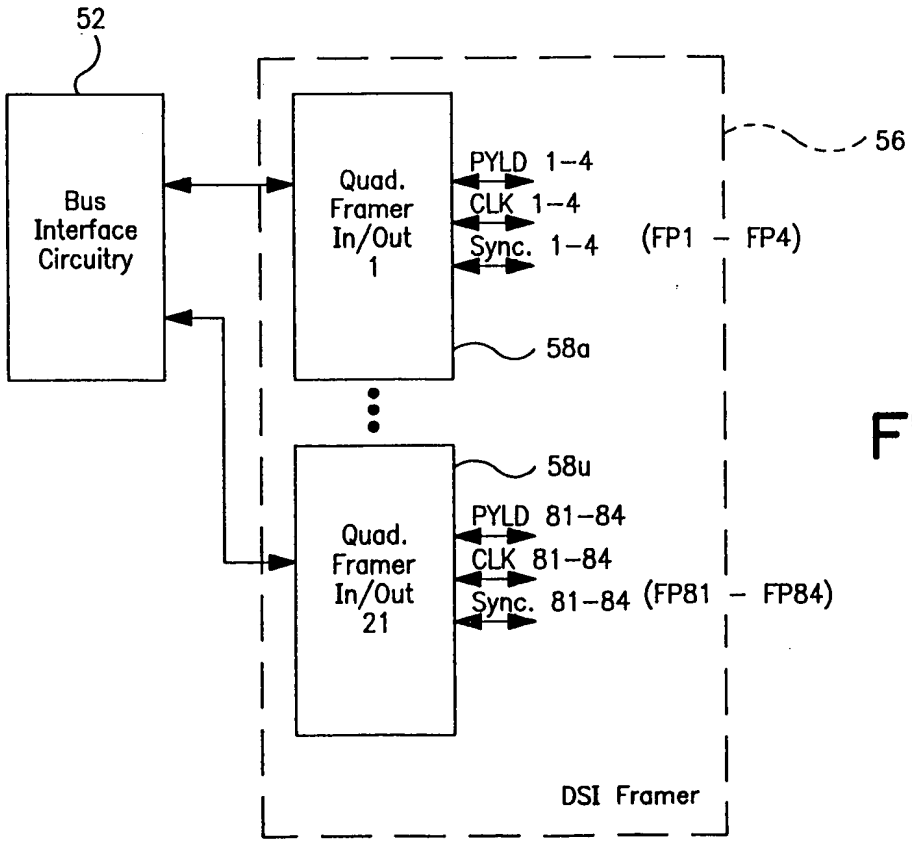
52
Bus Interface Circuitry
Quad. Framer In/Out 1
PYLD 1-4
CLK 1-4
Sync. 1-4
(FP1 - FP4)
56
58a
58u
Quad. Framer In/Out 21
PYLD 81-84
CLK 81-84
Sync. 81-84
(FP81 - FP84)
DSI Framer

FIG. 3a

09837 "SEQUENCE

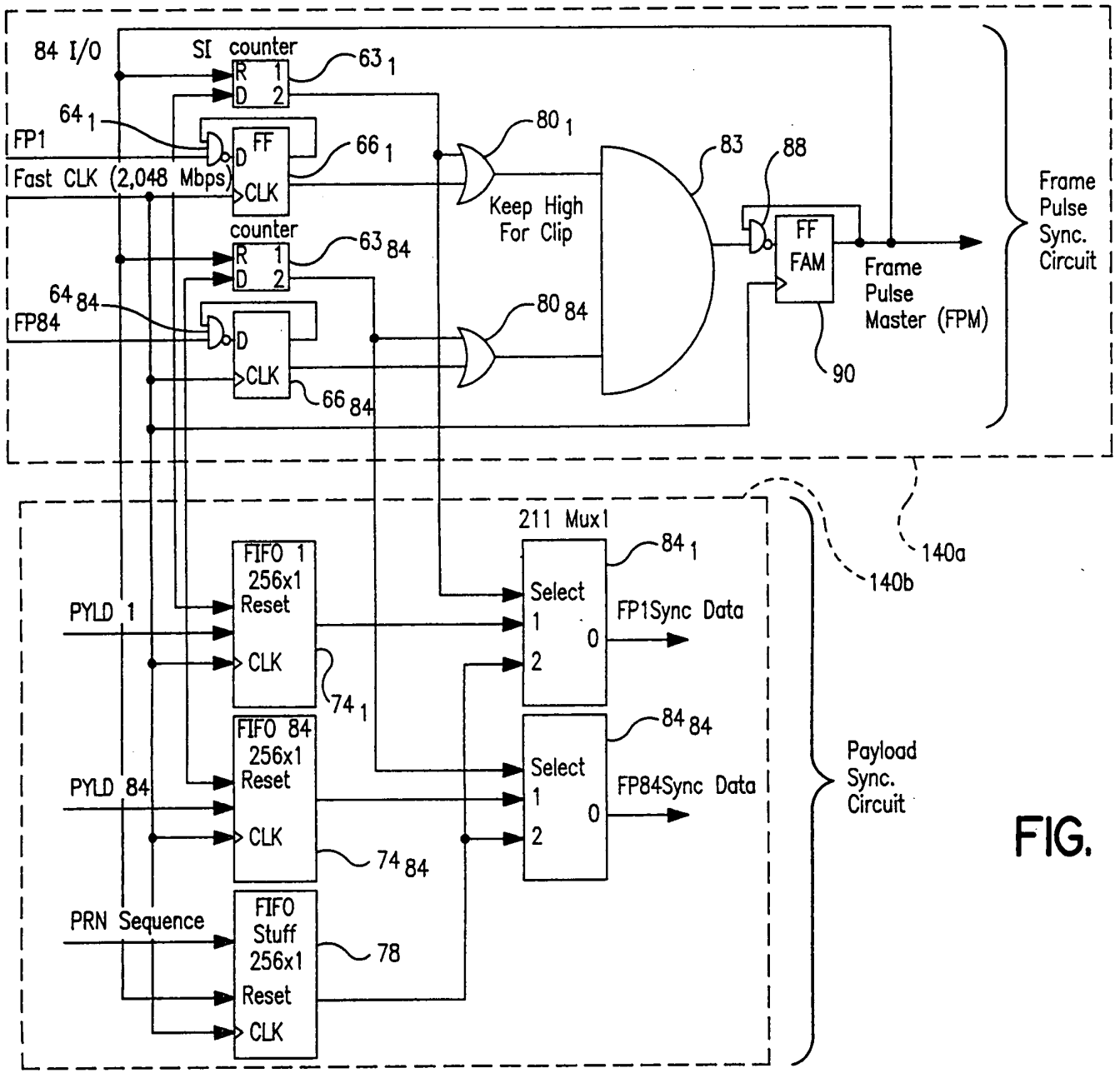

FIG. 4

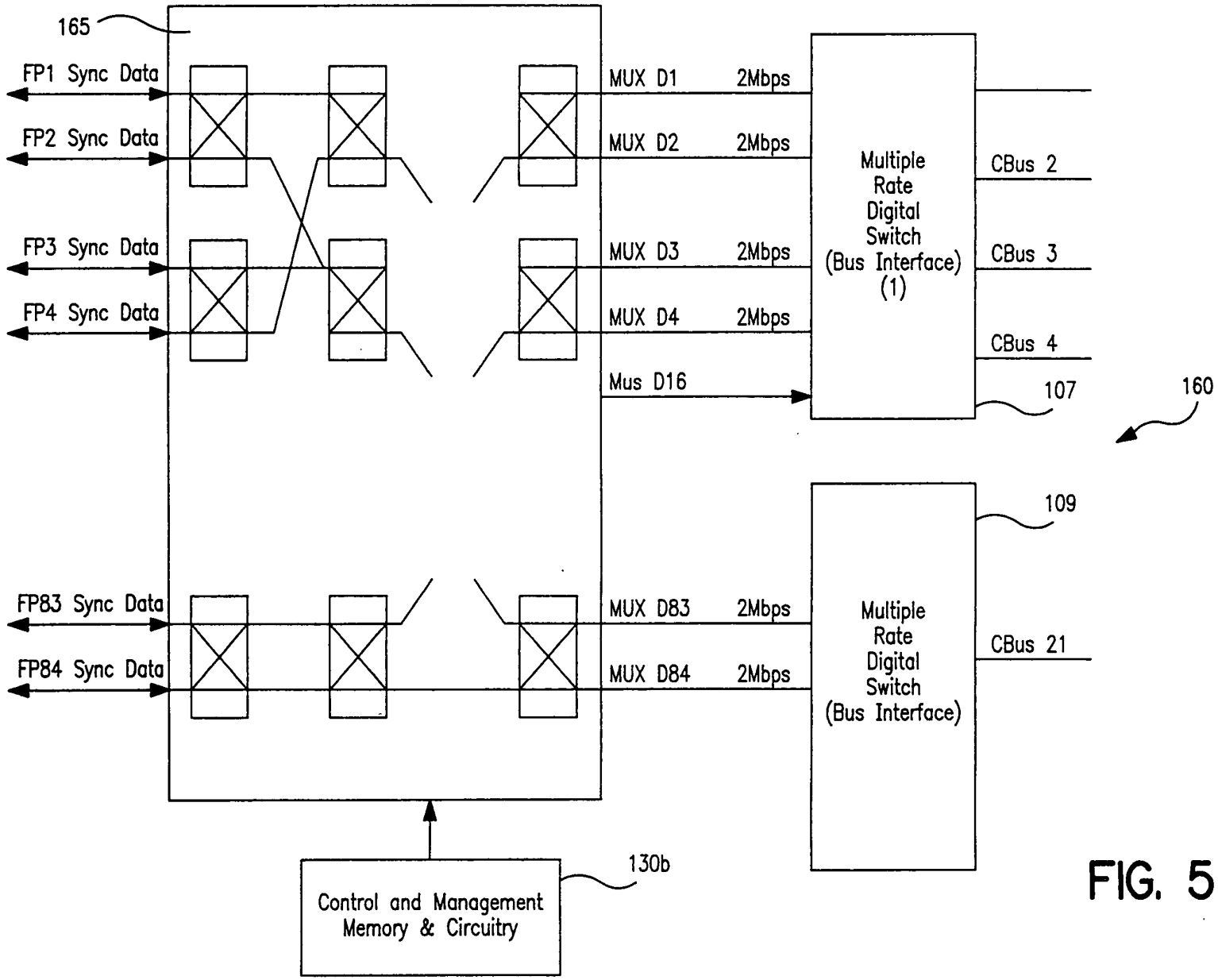
165
FP1 Sync Data
FP2 Sync Data
FP3 Sync Data
FP4 Sync Data
FP83 Sync Data
FP84 Sync Data
MUX D1 2Mbps
MUX D2 2Mbps
MUX D3 2Mbps
MUX D4 2Mbps
Mus D16
MUX D83 2Mbps
MUX D84 2Mbps
Multiple Rate Digital Switch (Bus Interface) (1)
CBus 2
CBus 3
CBus 4
107
160
109
Multiple Rate Digital Switch (Bus Interface)
CBus 21
130b
Control and Management Memory & Circuitry

FIG. 5

09262P 962812C9

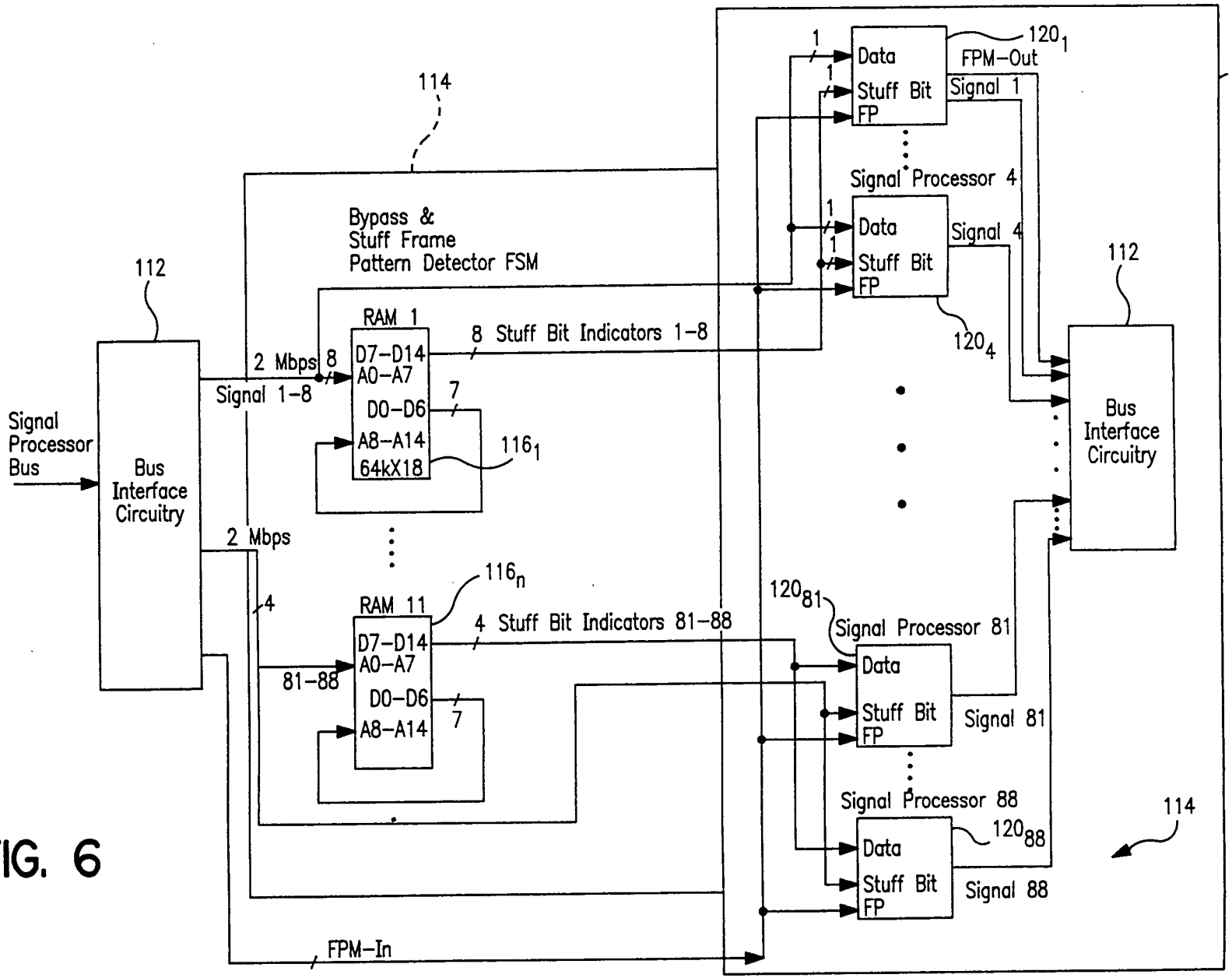

FIG. 6

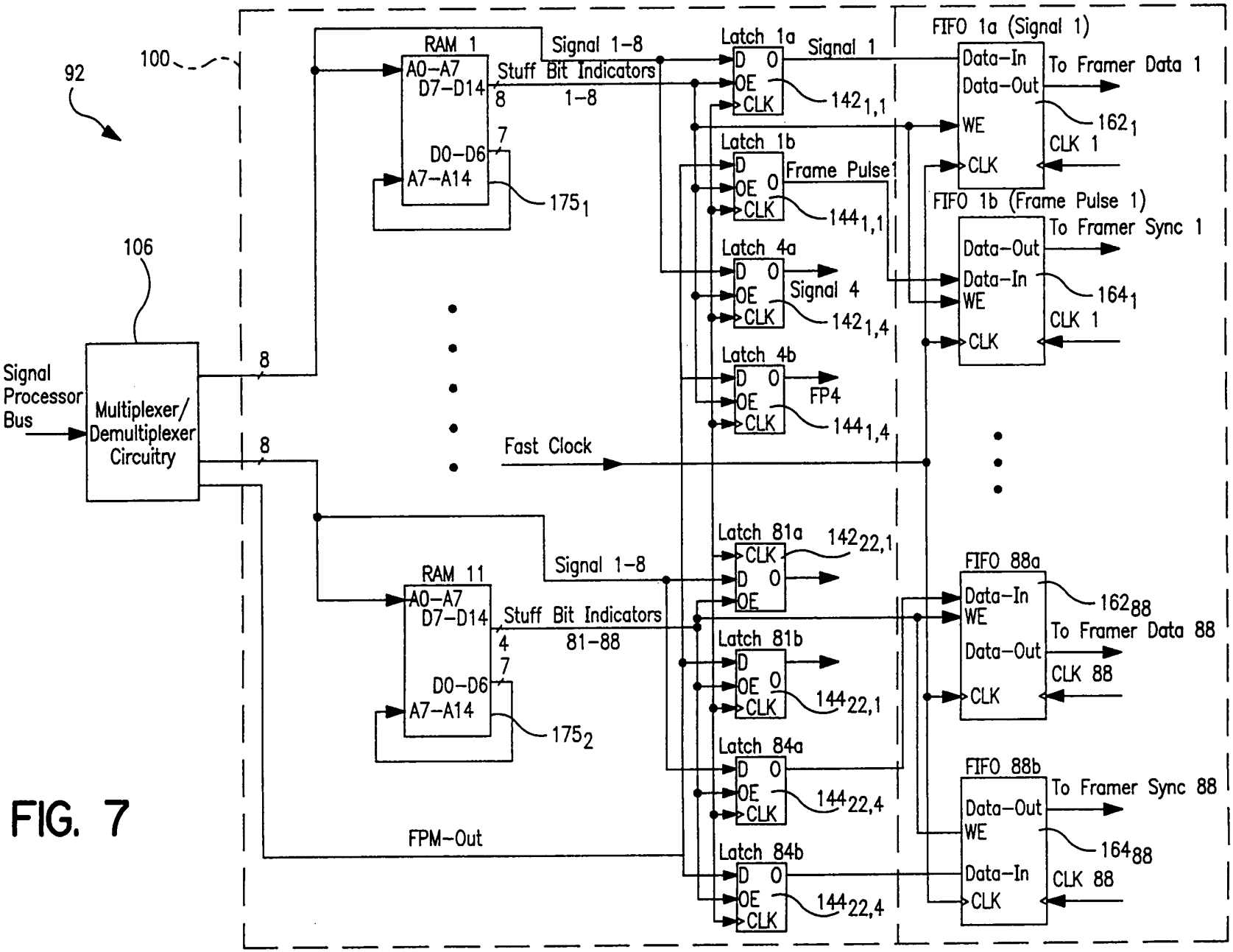
92
100
106
Signal Processor Bus
Multiplexer/ Demultiplexer Circuitry
8
8
RAM 1
A0–A7
D7–D14
DO–D6
A7–A14
Signal 1–8
Stuff Bit Indicators
1–8
8
7
175_1
RAM 11
A0–A7
D7–D14
DO–D6
A7–A14
Signal 1–8
Stuff Bit Indicators
81–88
4
7
175_2
Fast Clock
FPM–Out
Latch 1a
Signal 1
$142_{1,1}$
Latch 1b
Frame Pulse 1
$144_{1,1}$
Latch 4a
Signal 4
$142_{1,4}$
Latch 4b
FP4
$144_{1,4}$
Latch 81a
$142_{22,1}$
Latch 81b
$144_{22,1}$
Latch 84a
$144_{22,4}$
Latch 84b
$144_{22,4}$
D
OE
CLK
FIFO 1a (Signal 1)
Data–In
Data–Out
WE
CLK
To Framer Data 1
162_1
CLK 1
FIFO 1b (Frame Pulse 1)
To Framer Sync 1
164_1
CLK 1
FIFO 88a
162_{88}
To Framer Data 88
CLK 88
FIFO 88b
To Framer Sync 88
164_{88}
CLK 88

FIG. 7